SAT Control System

VIRGO

Weekly Meeting
January 31st, 2012

Meeting Agenda

- Running activities status report (all)
- Control System Architecture (A.Gennai)
- Development plan (A.Gennai)
- Mode Cleaner activities (A.Gennai)
- AOB

Control System Architecture

- Summary
  - Goals and requirements
  - Conceptual/Preliminary Design

Goals & Requirements

- Virgo/Virgo+ was a success! (from suspensions point of view)
  - Duty cycle extremely high (few hours off in more than 10 years of operation)
  - Virgo sensitivity never limited by our system.
  - Two major updates (coil drivers and DSPs) almost transparent to operation.
- Why are we talking about a new control system?

Goals

- Replace
  - Obsolete and old components
    - Boards have been running for years therefore MTTF is now too short to start a new decade (unless we start replacing all capacitors and chips)
- Reduce
  - Number and type of boards.
  - Analog signal path length.
  - Connections along the signals path.
  - Power.
- Improve
  - Reliability, operability and maintenability.

Requirements

- Not so many changes:
  - Tiltmeters (t.b.c.)
  - Piezos (today confirmed)
  - Filter #7 Control (6 d.o.f.)
  - Marionette Control (4 d.o.f)
  - Higher closed loop bandwidth for signal recycling operation → much shorter delays → much higher sampling rate (100 kHz – t.b.c. very preliminar)
  - Something still pending since a few years related to software (bugs, supervisor, separate dsp code and parameters, better GUI, data processing, ...)

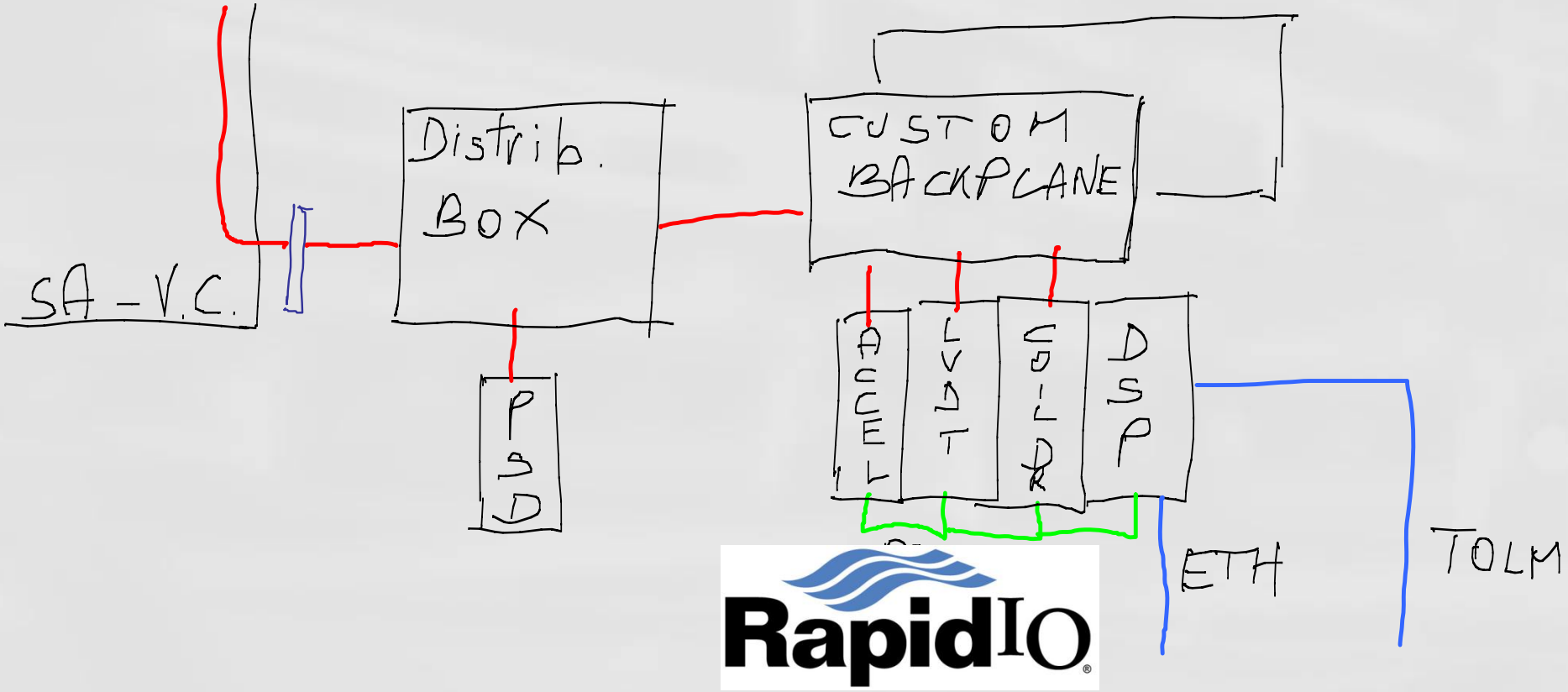
Conceptual Design

- New DSP
  - DSP know how is crucial for Virgo: we MUST develop a new DSP every few years
  - Connectivity no longer adequate
  - TMS320C6678
    - Eight TMS320C66x DSP Core Subsystems
    - 320 GMAC/160 GFLOP @ 1.25GHz
    - Four Lanes of SRIO 2.1 - 5 Gbaud Per Lane Full Duplex
    - Two Lanes PCIe Gen2 - 5 Gbaud Per Lane Full Duplex
    - Ethernet MAC Subsystem - Two SGMII Ports w/ 10/100/1000 Mbps operation
    - 64-Bit DDR3 Interface (DDR3-1600)

Conceptual Design

- Merge front-end electronics with data conveters
- Few boards to be developed
  - LVDT Readout
  - Accelerometer Readout
  - Coil Drivers
  - DSP
  - Custom backplanes and power supply
- Motor Control → INFN Trento/Padova
- Piezo Control →Physik Instrumente

Sketching …


SA - V.C.
Distrib. Box
PSD
CUSTOM BACKPLANE
ACEL
LVDT
GILDR
DSP
ETH
TOLM
RapidIO

…[continued]

- All electronics in Eurocard 6U crates located next to the tower.
- No CPU (RIOs)
  - Direct communication with DSP via Ethernet
- No VME
  - Communication among boards via RapidIO

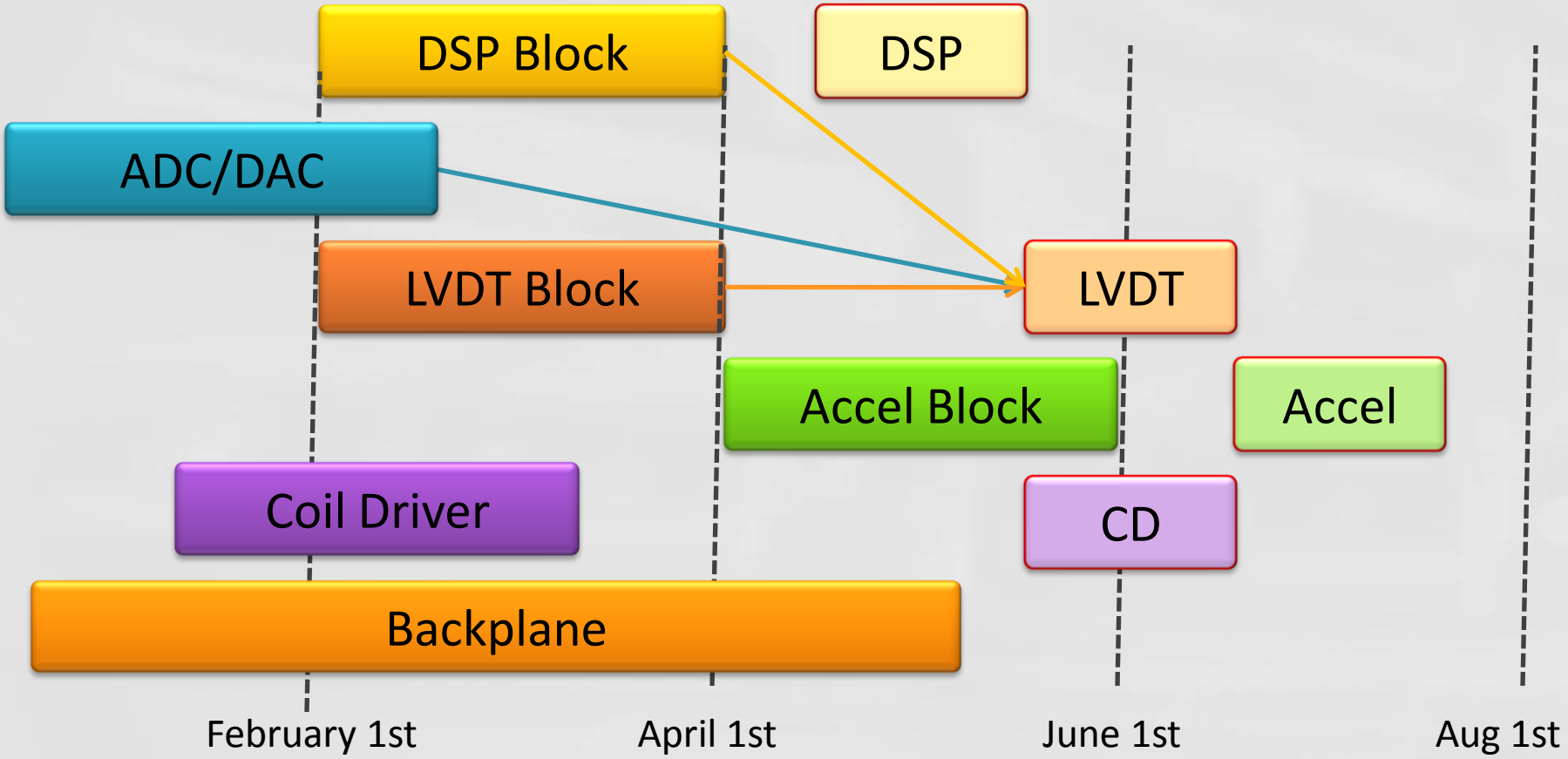
Reuse Blocks

- Each board is composed by a small subset of basic blocks
  - DSP block
    - Supervising, processing and communication
  - Data Conversion block
    - ADC-DAC + controlling FPGA and basic analog circuits
  - Analog block
    - Specific for each board

Development Plan

- Manpower
  - INFN Pisa – 3-4 FTE
  - EGO – 0.5 FTE (t.b.c.) + 1 FTE (software, t.b.c.)
  - Poland ???
- Organization
  - Each “Reuse Block” has one supervisor
  - Board merging by fewer persons (Alberto, Carlo)
  - Extensive use of firms for components procurement, assembly and preliminary tests.

Short Term Planning



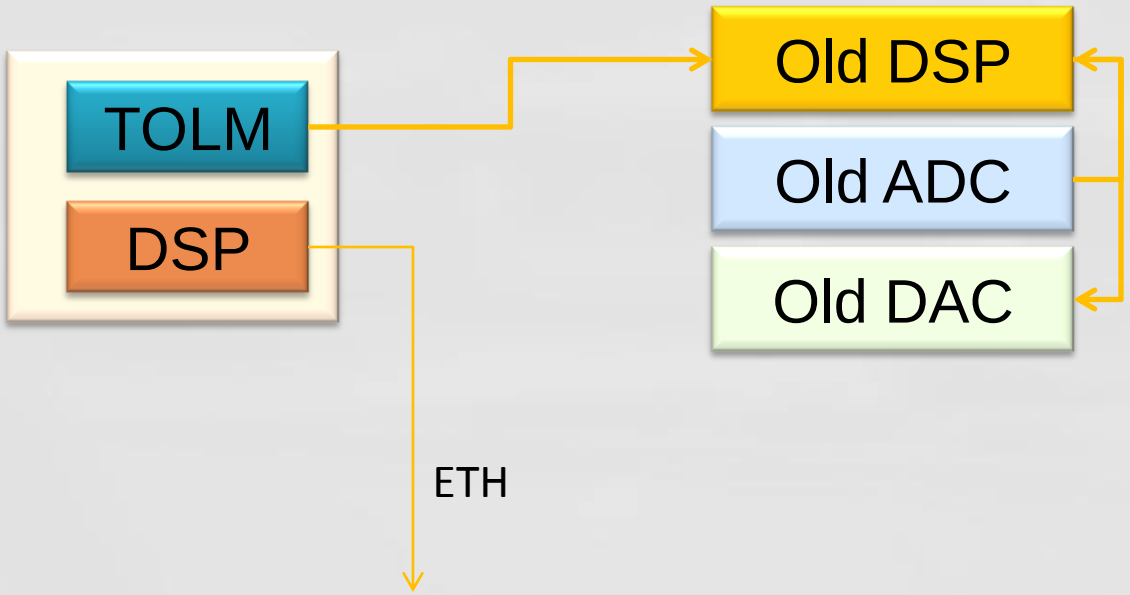
- All orders out within the end of July (2012 ☺)

Mode Cleaner
Tentative installation plan

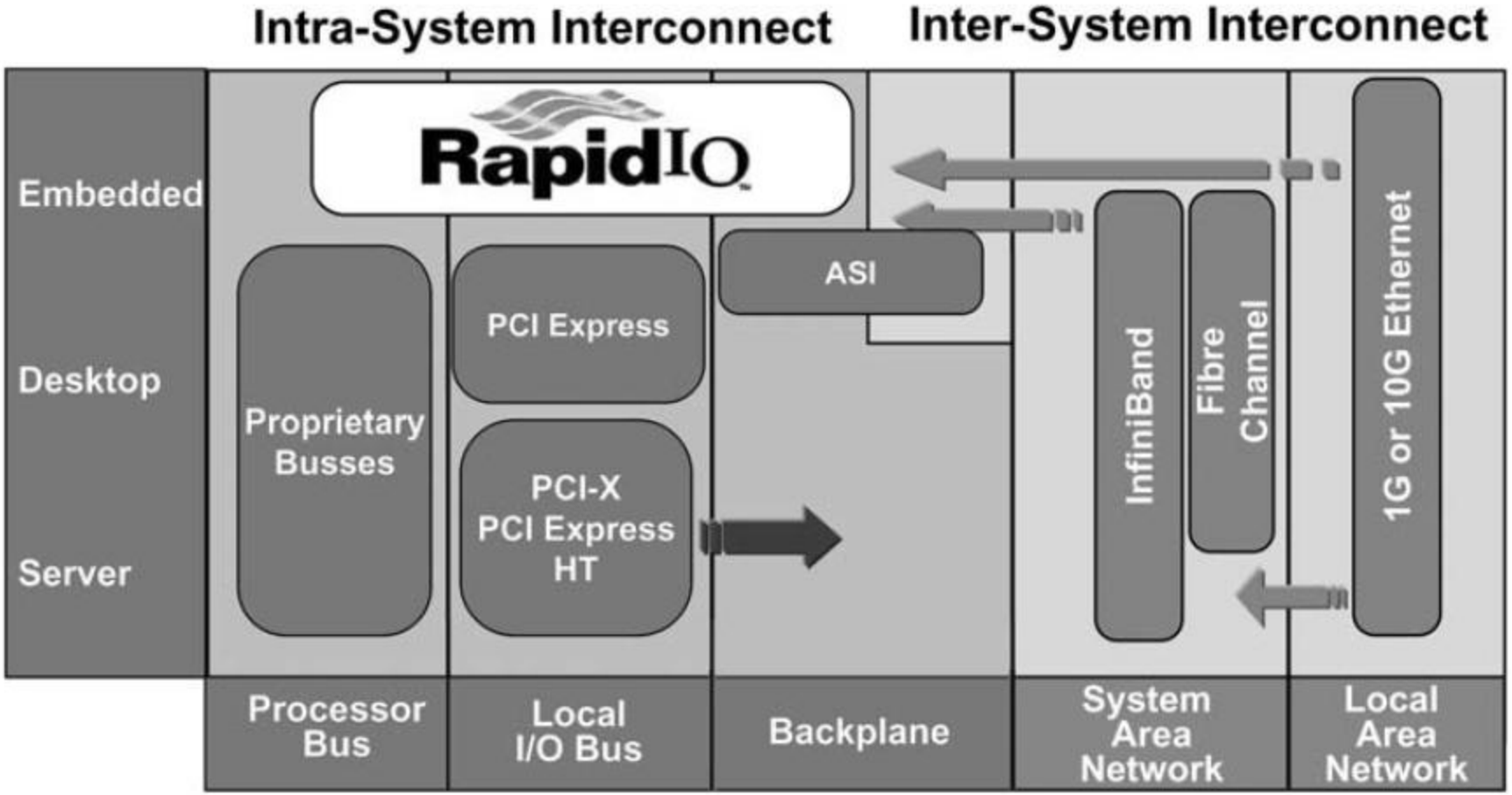
- MC activities will start in March (t.b.c.)
  - Need LVDT readout during SA disassembly
  - Need a first control unit within the end of 2012
  - Test piezo (t.b.c.)
  - Test F7 sensors/actuators(t.b.c.)
  - ...
- So many things to do, so little time ....

Prototype DSP carrier

- Development of a carrier board for a commercial DSP mezzanine and one TOLM



RapidIO


Intra-System Interconnect
Inter-System Interconnect
RapidIO
Embedded
Desktop
Server
Proprietary Busses
PCI Express
PCI-X
PCI Express
HT
ASI
InfiniBand
Fibre Channel
1G or 10G Ethernet
Processor Bus
Local I/O Bus
Backplane
System Area Network
Local Area Network