Minutes of Meeting

SAT Control System - Weekly Meeting
Tuesday, February 28th, 2012
11.00 - 13.00
EGO – New Council Room (Main Building)

Meeting Agenda

- Status Report
- LVDT (all)
- Coil Driver (all)

Participants

A.Gennai (AGE), C.Magazzù (CMA), D.Passuello (DPA), F.Nocera (FNO), F.Paoletti (FPA), R.Cavalieri (RCA), N.Grilli (NGR), R.Passaquieti (ROP), V.Dattilo (VDA)

Minutes

Pending Actions

Due to superposition with VirgoWeek, it was decided to postpone by one additional week pending actions hereafter listed.

1. ACT#3 (EMA/PRU – 1 wk) Estimate max forces and check max current
2. ACT#4 (AGE – 1 wk) Check what was injected during calibration.
3. ACT#5 (VDA – 1 wk) Talk with vacuum people and select a preliminary value for peak temperature and 10 minutes rms temperature.
4. ACT#6(AGE- 3 wks) Make a preliminary evaluation of perfor
5. ances and cost of 'heat pipe' cooling systems.

Running Activities

STA#1(CMA) Power supply prototype board is ready to be test

DEC#1(all) Test will begin in the next days and include programming Digital Signal Controller used to read temperature probes.

ACT#1(CMA,AGE,RPA – 2 wks) Complete tests on power supply prototype including test in standard and custom aluminum crates.

LVDT

AGE presented a couple off slides showing a top level block diagram of new LVDT board and communication links between new DSP board and a generic analog interface board (Accelerometer, LVDT, Coil Driver …).

STA#2(AGE) ADC has a differential input requiring zero common mode voltage and max 6.4 Vpp. This statement applies to Coil Driver as well.

Coil Driver

STA#3(FPA) High power section, based on opamp OPA548, requires +/- 15V supplies due to high headroom required by operational amplifier.

STA#4(AGE). I think important to keep supply voltages as low as possible to minimize power and temperature.

STA#5(FPA) Also low noise part requires 3V headroom and therefore +/-15V is the best choice for power supply.

DEC#2(all). +/-15V will be adopted only if limiting low noise sections otherwise we will use +/-12V.

STA#6(AGE) ADC input is differential with zero Volt common mode.

DEC#3(all) Any analog system interfacing to ADC must provide the zero common mode balanced signal to drive ADC.

STA#7(AGE) We have 2 adc channels available. We need to decide what we can monitor.

DEC#4(all) one channel will be assigned to coil voltage readout.

STA#8(all) It looks like there is no need to have a low noise current monitor. We never used it in Virgo/Virgo+ and there are some problem for switching readout when switching from Hp to LN and vice versa.

DEC#5(all) the second channel will be assigned to the readout of voltage drop across a 0.1 Ohm resistor in series with the coil. Signal can be amplified by a factor between 6 and 10 before entering the adc.

Coil Temperature

STA#9(VDA) Tests are undergoing for evaluate the maximum allowable temperature in a coil in vacuum. Tests try to evaluate temperature and time needed to deposit a monolayer onto mirrors. Results will be available soon.

Next Meeting

Next meeting will be dedicated to COIL DRIVER and we suppose we are able to close pending actions.

Actions Summary

See pending actions at the beginning of this document.

Decisions Summary

DEC#1(all) Test will begin in the next days and include programming Digital Signal Controller used to read temperature probes.

DEC#2(all). +/-15V will be adopted only if limiting low noise sections otherwise we will use +/-12V.

DEC#3(all) Any analog system interfacing to ADC must provide the zero common mode balanced signal to drive ADC.

DEC#4(all) One channel will be assigned to coil voltage readout.

DEC#5(all) the second channel will be assigned to the readout of voltage drop across a 0.1 Ohm resistor in series with the coil. Signal can be amplified by a factor between 6 and 10 before entering the adc.