Minutes of Meeting

SAT Control System - Weekly Meeting
Tuesday, February 14th, 2012
11.00 - 13.00
EGO – New Council Room (Main Building)

Meeting Agenda
- Approval of last meeting minutes (all - 2 minutes)
- Running activities status report (all)
- Feed through pinout: present and future (V.Dattilo)
- Suspension crates connectors pinout (R.Paoletti/A.Gennai)
- Discussion

Participants

A.Gennai (AGE), C.Magazzù (CMA), F.Carbognani (FCA), F.Nocera (FNO), F.Nenci (FNE), F.Paoletti (FPA), G.Ballardin (GBA), M.Bitossi (MBI), R.Cavalieri (RCA), R.Paoletti (RPA), V.Dattilo (VDA)

Minutes

FPGA
STA#1 (MBI) (Reply to last meeting ACT#1) Altera Serial RapidIO Gen1 and Gen2 IP are both compatible with TMS320C6678 DSP
DEC#1 (all) We will implement SRIO communication link between DSP and FPGA using Altera IP.
DEC#2(all) (Reply to last meeting ACT#1) Carrier prototype needs to use Cyclone IV GX30 since it has both transceivers for SRIO and adequate number of I/O pins (290).
STA#2(MBI) Still tbd the number of IO pins for Data Conversion block FPGA.
DEC#3(all) Data Conversion block will use Cyclone IV GX FPGA
ACT#1(MBI-1 wk) Fix number of IO pins and choose FPGA for Data Conversion Block.

Coil Driver
DEC#4 (all) Minutes of last meeting have been updated adding one decision: maximum output voltage is 10V peak.

Suspension Tower – Suspension Crates Cabling
V. Dattilo presented feed through description (slides https://workarea.ego-gw.it/ego2/virgo/mirror-suspension-control/advanced-virgo-suspension-control-systema/weekly-meeting-slides-mom/Feedthrough_SATCS_14feb12.doc)
STA#3(VDA) Number of devices in a long tower will grow up to about 100 (from 77). Estimated total number of FT pins is 378+145.
STA#4(VDA) All Feed Though are on 32 pin connectors MIL-C-26482
STA#5(VDA) Each tower has a different FT configuration.
STA#6(VDA) All FT are distributed on 3 different flanges. Two at 'technical virole' level and one at base level.
STA#7(VDA) Each cable connects different devices located close one to the other.

DEC#5 (all) We will have the same FT connectors on all towers (same signals) even if in different locations (in general different flanges).

STA#8(FNO) At present there is no idea about cable trays for cabling between suspension and suspension crates.

A.Gennai presented few slides with a tentative description of the new suspension control crated (slides: https://workarea.ego-gw.it/ego2/virgo/mirror-suspension-control/advanced-virgo-suspension-control-systema/weekly-meeting-slides-mom/SAT-CS_Weekly_140212.pdf)

STA#9(AGE) Basic architecture foresees two crates. One devoted to top stage and chain control (21 signals) and one for bottom stage control (28 signals). Crates will be 12 slot.

STA#10(FPA) Power dissipation in coil driver can be an important issue. We will need large heat sinks and very likely forced air flow.

Follows a preliminary discussion on how implementing cabling but today we have not enough elements to define most of the details.

DEC#6 (all) No more than 4 cables shall arrive to each crate. At present we foresee about 10-12 signals per cable. Signals will be connected to backplanes via a small PCB that will allow routing all wires (solded or screwed on PCB).

DEC#7 (all) It is required to have the possibility to assemble cables in laboratory.

Next Meeting

During next meeting we will concentrate on the few actions pending about coil driver.

Actions Summary

No specific actions. We have a few pending actions from previous meeting (deadline updated).

1. <u>ACT#3 (EMA/PRU – 1 wk)</u> Estimate max forces and check max current
2. <u>ACT#4 (AGE – 1 wk)</u> Check what was injected during calibration.
3. <u>ACT#5 (VDA – 1 wk)</u> Talk with vacuum people and select a preliminary value for peak temperature and 10 minutes rms temperature.
4. <u>ACT#6(AGE- 3 wks)</u> Make a preliminary evaluation of performances and cost of 'heat pipe' cooling systems.

Decisions Summary

DEC#1 (all) We will implement SRIO communication link between DSP and FPGA using Altera IP.

DEC#2(all) (Reply to last meeting ACT#1) Carrier prototype needs to use Cyclone IV GX30 since it has both transceivers for SRIO and adequate number of I/O pins (290).

DEC#3(all) Data Conversion block will use Cyclone IV GX FPGA

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