Minutes of Meeting

SAT Control System - Weekly Meeting
Tuesday, February 7th, 2012
11.00 - 13.00
EGO – New Council Room (Main Building)

Meeting Agenda
- Running activities status report (all)
- Coil Driver global architecture and new naming conventions (A. Gennai)
- Coil Driver Requirements (F. Paoletti)

Participants

A.Gennai (AGE), C.Magazzù (CMA), D.Passuello (DPA), E.Majorana (EMA), F.Carbognani (FCA), F.Frasconi (FFR), F.Nocera (FNO), F.Paoletti (FPA), G.Ballardin (GBA), G.Vajente (GVA), M.Bitossi (MBI), P.Ruggi (PRU), R.Cavalieri (RCA), R.Paoletti (RPA), R.Passaquieti (ROP), V.Dattilo (VDA),

Minutes

No pending actions from previous meeting.

Note: actions and decisions list are summarized at the end of this document.

FPGA

The meeting was preceded by a restricted session (AGE, CMA, DPA, MBI, RPA) mainly dedicated to FPGA choice for the prototype DSP carrier board being developed by RPA. During this session we had the following conclusions.

ACT# 1(MBI – Feb 10) Check differences between Altera Serial RapidIO GEN1 and GEN2 and check compatibility with TI DSP SRIO interface.
DEC#1 (all) We need to move from Cyclone IVE to Cyclone IV GX due to the lack of transceivers
ACT#2 (RPA/MBI – Feb 10) Select proper number of IO pins (150 ??) and choose FPGA.
STA#1 (CMA) Power Supply PCB ready. Mounting will start as soon as possible (few days delay to laboratory removal)

Coil Driver

AGE presented two slides with a high level description of the new coil driver board including a dsp block for communication, a data conversion block and the analog section (slides: https://workarea.ego-gw.it/ego2/virgo/mirror-suspension-control/advanced-virgo-suspension-control-systema/SAT-CS_Weekly_070212.pptx)

FPA presented top level requirements (slides: https://workarea.ego-gw.it/ego2/virgo/mirror-suspension-control/advanced-virgo-suspension-control-systema/AdVCD_FPA.ppt)

High Power Section

STA#2 (FPA) Superattenuator and payload coils have a dc resistance ranging from 10 up 25 Ohms (cabling included)
STA#3 (AGE) High power is essentially required by calibration. We should understand better motivations.

DEC#2 (all) People involved in SAT and PAY design should participate actively to actuators calibration.
STA#4 (PRU) High Power is required not only for calibration but also during standard commissioning activities.
STA#5 (EMA) Magnets on new marionette are smaller but we have more coils and lower frequency modes: we will need more or less the same current we used in Virgo+.
ACT#3 (EMA/PRU – 2 wks) Estimate max forces and check max current
ACT#4 (AGE – 2 wks) Check what was injected during calibration.
DEC#3 (all) We need High Power
DEC#4 (all) 1 A max current is a reasonable value
STA#6 (FPA) At marionette level since dc resistance is about 20 Ohms, maximum current will be 0.5A.
STA# 7(EMA) New coils will have a dc resistance of 9 ohm while old one were about 13 ohm for a maximum current in the 0.75A range (acceptable).
DEC#4A (all) Where coil + cable impedance is larger than 10 Ohms (f7-marionette) maximum current can be reduced to 0.7-0.75A.
STA#8 (FPA) Ok for 1 A maximum current but this implies about 10W to be dissipated by the coil.
STA#9(VDA) In the past we checked that 1A dc current produce in few minutes a temperature in the 150 C range. It is known that at such temperature kapton outgassing increases by two orders of magnitude. This could be dangerous for mirrors even if we have no data about this.
STA#10(EMA) This point is today more relevant since F7 coils will be now below the separating roof.
DEC#5 (all) We need to fix a maximum temperature for the coil (peak and rms over a given amount of time).
ACT#5 (VDA – 2 wks) Talk with vacuum people and select a preliminary value for peak temperature and 10 minutes rms temperature.

Low Noise Section

STA#11 (PRU) LN1 and LN2 are useful while we do not see the need for LN3 and LN4
DEC#6(all) LN3 and LN4 will be implemented only if cost is negligible.
STA#12(EMA) PAY is investigating the possibility to reduce magnets on mirrors by a factor 3. Of course this will demand more current.

Power Dissipation

STA#13(FPA) Coil driver analog section will dissipate about 3W/channel at zero output current/voltage. This amount should be added to the amount required by digital part: probably we will not be able to operate without fans.
STA#14(ROP) We can take into account the possibility to use heat pipes (tubi di calore) to take out heat from boards.
ACT#6(AGE- 1 month) Make a preliminary evaluation of performances and cost of ‘heat pipe’ cooling systems.

Bandwidth

STA#15(GVA) Signal recycling will require a closed loop bandwidth in the 200-400 Hz range. This implies a total delay in the range 50 to 100 microseconds (today is about 650) including the 16 usec transport delay between central building and terminal towers (max total delay is computed assuming 10 degrees as maximum additional phase shift at unity gain frequency)
STA#16(AGE) We modified DAC design to have a delay in the 5 usec range.
DEC#7(all) New coil drivers shall have a group delay not larger than 5 usec (that is about 30 kHz assuming a single pole lowpass transfer function)
STA#17(FPA) Not easy achieve such performances in HP section.

Power Supply

STA#18(AGE) In order to evaluate supply requirements it would be useful knowing what is the maximum number of coils that can be driven with 1A simultaneously on the same payload.

STA#19(PRU-GVA) Reply: one degree of freedom that is from 2 to max 4 coils.
DEC#8(all) supply shall allow from 4 to 8 A per payload.

Monitoring

STA#20(AGE) Monitoring must be reduced to no more than 2 channels to reduce number of on board ADC
DEC#9(all) We will monitor output voltage (voltage applied to the coil) and output current. In HP current is read measuring voltage drop across a small resistor (same as Virgo+). After switch to LN current is monitored measuring voltage drop across series resistance.

Next Meeting

DEC#10(all) Next meeting will be dedicated to the 'distribution box' that is analog cabling (in air) between Superattenuator and suspension control crates.
ACT#7(VDA – 1 wk) Prepare 1-2 slides with feed through pin-out
ACT#8(AGE/RPA -1 wk) Prepare 1-2 slides with proposed crate connectors' pin-out.

Actions Summary

1. ACT# 1(MBI – Feb 10) Check differences between Altera Serial RapidIO GEN1 and GEN2 and check compatibility with TI DSP SRIO interface.
2. ACT#2 (RPA/MBI – Feb 10) Select proper number of IO pins and choose FPGA.
3. ACT#3 (EMA/PRU – 2 wks) Estimate max forces and check max current
4. ACT#4 (AGE – 2 wks) Check what was injected during calibration.
5. ACT#5 (VDA – 2 wks) Talk with vacuum people and select a preliminary value for peak temperature and 10 minutes rms temperature.
6. ACT#6(AGE- 1 month) Make a preliminary evaluation of performances and cost of 'heat pipe' cooling systems.
7. ACT#7(VDA – 1 wk) Prepare 1-2 slides with feed through pin-out
8. ACT#8(AGE/RPA -1 wk) Prepare 1-2 slides with proposed crate connectors' pin-out.

Decisions Summary

1. DEC#1 (all) We need to move from Cyclone IVE to Cyclone IV GX due to the lack of transceivers.
2. DEC#2 (all) People involved in SAT and PAY design should participate actively to actuators calibration.
3. DEC#3 (all) We need High Power section.
4. DEC#4 (all) 1 A max current is a reasonable value.
5. DEC#4A (all)) Where coil + cable impedance is larger than 10 Ohms (f7-marionette) maximum current can be reduced to 0.7-0.75A (i.e. maximum voltage applied at coil is 10V peak)
6. DEC#5 (all) We need to fix a maximum temperature for the coil (peak and rms over a given amount of time).
7. DEC#6(all) LN3 and LN4 will be implemented only if cost is negligible.
8. DEC#7(all) New coil drivers shall have a group delay not larger than 5 usec (that is about 30 kHz assuming a single pole lowpass transfer function)
9. DEC#8(all) supply shall allow from 4 to 8 A per payload.
10. DEC#9(all) We will monitor output voltage (voltage applied to the coil) and output current. In HP current is read measuring voltage drop across a small resistor (same as Virgo+). After switch to LN current is monitored measuring voltage drop across series resistance.
11. DEC#10(all) Next meeting will be dedicated to the 'distribution box' that is analog cabling (in air) between Superattenuator and suspension control crates.