EGO R&D program on Gravitational Wave Detection

Final report

R&D for the Electronic Upgrade

Part I
Timing; TOLM, ADC; Analog Electronic

LAPP Annecy

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1 Participants

[List the scientists/engineers/students that have worked on the project]

Name	*Laboratory*	*Position*	*Involvement time (%)*
Thierry. Bouedo	LAPP	Staff (software engineer)	100%
Olivier Chautemps	LAPP	Student (electronic)	9 months in 2004
Sonia Karkar	LAPP	Post doc (timing system)	70% (+30% det. support)
Nicolas Letendre	LAPP	Staff (electronic engineer)	100 %
Alain Masserot	LAPP	Staff (software engineer)	20 %
Benoit Mours	LAPP	Staff (physicist)	10 %
Jean Marc Nappa	LAPP	Staff (electronic)	100%
Gérard Levanic	LAPP	Student (electronic)	6 months in 2006
Yoan Maulaz	LAPP	Student (electronic)	3 months in 2006
Emmanuel Paccaud	LAPP	Staff (software engineer)	90 % since Jan. 2006
Julie Prast	LAPP	Staff (electronic engineer)	20% in 2004
Sébastien Vilalte	LAPP	Staff (electronic engineer)	30%

2 Description of the project as funded

[Describe the project as it was initially proposed and funded]

The reasons for studying the electronic upgrade were:

- Obsolete electronic: The modules were designed more than 10 years ago and components do not any more exist. This limits the evolution of the current system (difficulty to add more channels or control loops) or could be dangerous for the long term reliability
- Not enough computing power. This is the case at all level,
  - sensing (photodiode readout, or other readout that require more specific filters)
  - global control were more complex algorithm are needed
  - local controls (processing done on a VME CPU)
  - mirror and suspension control (DSP)
- Improve the control bandwidth for more stable control: This require to increase the frequency of the loop (currently 10kHz for the main loop) and/or reduce the number of elements in the pipeline (like doing the photodiode processing + global control in the same CPU) to reduce the delay of the loop. To achieve such a result it is mandatory to replace the VME bus by a faster bus for the data transfer (PCI and DSP link ports)
- More robust timing system with the distribution to the GPS time to all processing units for a more reliable data taking and flexible system.
- Improve the dynamic of the sensing (analog electronic and ADC) and the actuation (DAC and coil drivers).

The main part of the project

Currently the Virgo real time control system and it's associated data acquisition system is a distributed control system over more than 40 VME crates where we can see 4 main task

- A timing system that synchronized all the sensing and control parts and provide an absolute time stamp for the data collection.
- The communication between the different components done with specific low latency module, the Digital Optical Link (DOL) (plus the slow control done Via Ethernet)
- The sensing with the different photodiodes, local control, LVDT or auxiliary channels like seismometers.
- The real time computing done in VME processors (RIO) and DSPs.
- The actuation like the coil drivers

The developments made by the Annecy group cover the first four items with some overlap for the EGO/Pisa group for the third and fourth ones.

3 Accomplishments

3.1 Project organization/Introduction

The first part of the project was to define the individual components to be build with a special emphasis on the communications boards since they are providing the interface to all modules. This overall architecture has been described in [2]. The Figure 1 describes the main step of the control loop.

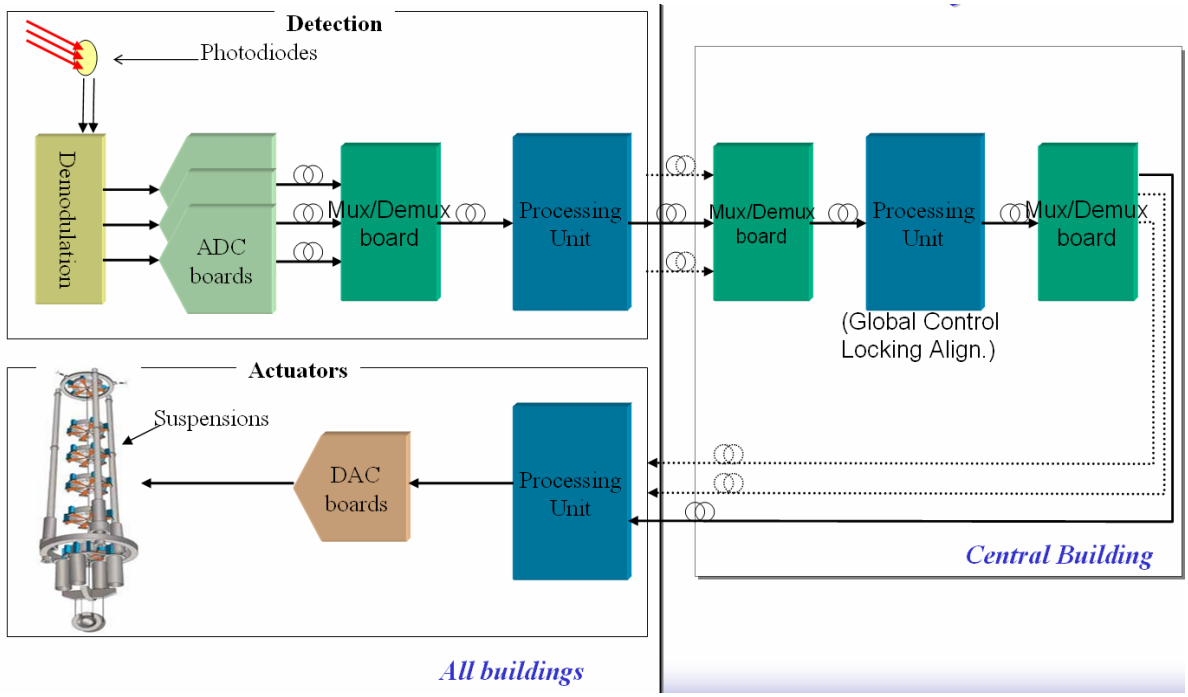

Figure 1 Schematic of the main Virgo control loop

Therefore we identify the following task

1. Timing and Optical Mezzanine (TOLM) This is the basic communication module that provide two couples of optical transmitters (2 in and 2 out) plus the timing signals. Data could be send to the PCI bus and DSP link ports and therefore this module could be used in the custom Virgo DSP or in plain PCs. This is the glue between all the module/crate of the Virgo overall control system. It is usually a PMC module, but smaller version of its design are foreseen to be integrated in a the ADC and DAC modules.
2. The timing system. This is the GPS receiver plus all the components needed to distribute the timing signal to all the TOLM modules. This has been split in two activities:
    a. The GPS receiver
    b. The timing distribution system
3. The MUX/DMUX board. This is a fan out module that let the system be organized in star configuration for instance (different ADC modules going to the single global control processor and then going to the different suspension controls).
4. The ADC board
5. The analog conditioning board
6. The DSP mezzanine (not described in this report)
7. The DSP/TOLM motherboard (not described in this report)

8. The DAC board (not described in this report)

As it has been said, the scheduled followed in this development was to first focus on the interface module, the TOLM, then develop prototypes of all the other elements in order to perform global tests before starting the production.

It must be added that the current development is not yet completed. A good fraction of these prototypes exist, but not all of them. They are expected to be available for this fall.

Since this is the development of new modules, the results are linked to the work performed and therefore the following sections will described the accomplishments (work and results) for each of the above elements. It will be followed by a section describing the software development.

3.2 Timing system

3.2.1 Overall description

The goals of the new timing system are:

- Provide an absolute timing information (GPS time) to all elements and not just a frame number.
- Reduce the access speed for the timing information (GPS time and sampling number) for the element of the loop.
- Increase the flexibility in the shape of the timing pulse.
- Replace the old components, especially the master clock by new modules.
- Reduce the electromagnetic noise.
- Be a robust and reliable system.

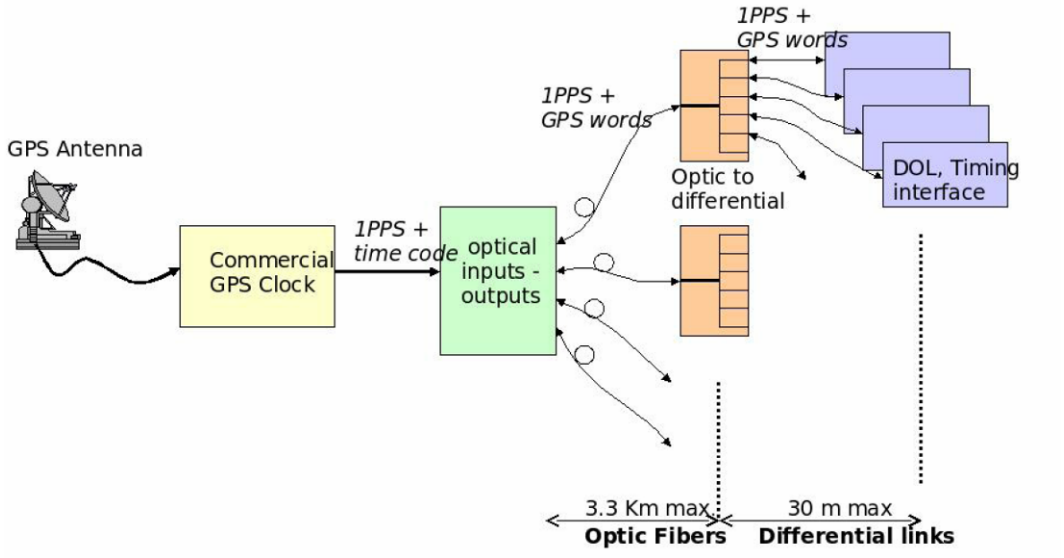

Figure 2 Overall view of the timing system

The Figure 2 presents the schematic of the new timing system. Like the current one, it is a star system starting from a master clock with fibber going to all “users” modules, (usually a TOLM). However, the number of signal distributed will be limited to two signals (instead of four now):

- A one pulse per second (1PPS) signal for the local clock synchronization with absolute timing information encoded using the IRIG-B protocol. The 1PPS signal will be used to synchronize a local oscillator located on the user's module.
- A fast clock (10MHz) to be use when the user modules do not have a local clock. This will provide some cost saving but put additional requirement on the jitter of the timing distribution. This jitter should be less than 0.1 ns if we do not want that a 10 kHz line that fill the full dynamic range of a 16 bits ADC introduce additional noise [1].

To reduce the electromagnetic noise, the optical fibers will go up to the racks and differential signals be used up to the users module instead of TTL signal in coaxial cables.

3.2.2 Master GPS clock

A market survey was conducted in 2005 to search for suitable GPS receiver that provide GPS timing in the IRIG-G frames as well as clock status information [8]. Following a call for tender, a signal generator SW1050-R-10 from MicroSystems with a GPS Motorola M12T receiver and a Rubidium clock has been selected. The clock arrived in December 2005 and tests started.

To perform the test, the IRIG-B frames were recorder at 20 kHz during days to check the validity of the GPS time and auxiliary information. Some problems were observed:

- The quality bits specifying if the clock was synchronized and GPS satellites or not were not present
- A few times per week, two IRIG-B frames were observed with the same GPS time.

These problems were fixed (upgrade of the firmware) and the test continued. Currently, no other problems have been observed on the GPS time on 3 weeks of data. But the tests will continue on a longer period and also with the comparison of the clock signals with an other atomic clock to check the absence of glitches.

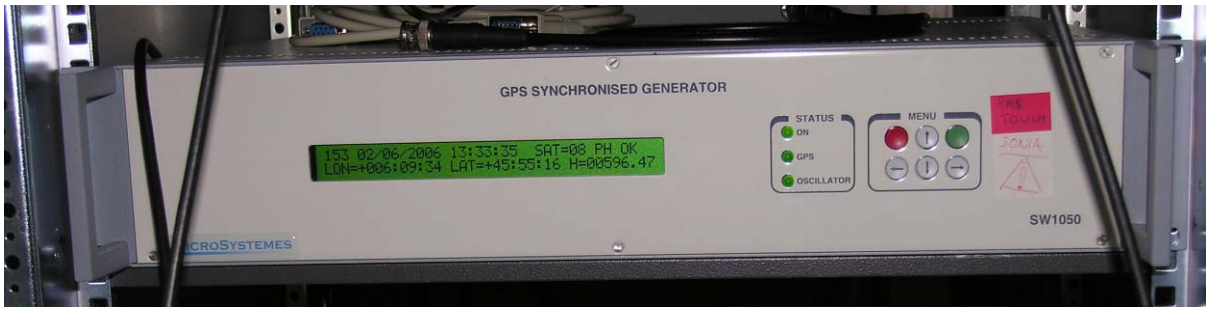

Figure 3 Front panel of the new GPS receiver

3.2.3 Timing Distribution Box (TDBox)

The market survey of the timing distribution [8] indicates a minimal cost of about 140,000 Euros, with a system that distribute only one signal (not the 10 MHz clock) and not differential output. In addition, they were not providing any guaranty about the jitter introduced in the timing distribution nor the long term maintenance of these components since not industrial standard exist for the distribution on optical fibbers. Therefore it was decided to develop a custom module, the TDBox.

The TDBox should receive input from the master GPS clock and provide multiple optical outputs or receive optical outputs and provide multiple differential outputs for all Virgo modules (see Figure 2). A single design has been made but two options for the somehow costly optical components will be used.

The first prototype has been designed and two modules have been build (see Figure 4 & Figure 5).

Figure 4 Front view of the TDBox prototype.
From left to right we can see the input BNC and RJ45 connectors (up to 4 electrical signals could be distributed), the source selector, the output RJ45 and BNC connectors.

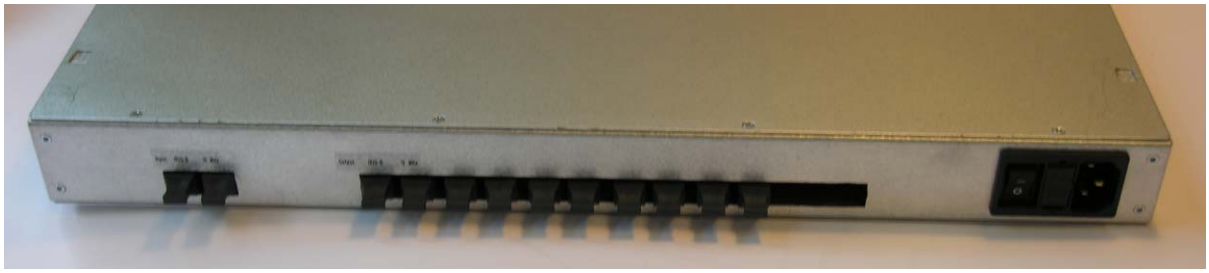

Figure 5 Back view of the TDBox prototype.
The two optical inputs are on the left and 5 couples of optical output are in the center.

Tests started with these two prototypes in early June 2006. The first global test was to send a TTL signal in a first box, that convert it to an optical signal while the second box convert it back to an electrical signal. By comparing this output to a signal that comes directly from the signal generator we can check the overall behavior of the box and measure the jitter in the time distribution. The Figure 6 present such a result were a jitter of 18 ps has been observed, meeting our specification.

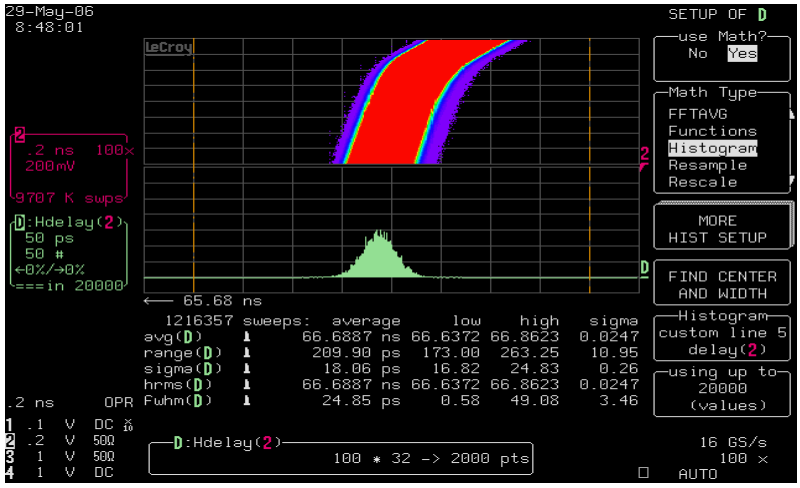

Figure 6 Jitter introduced by two TDBox connected using an optical fiber.

More extensive test will continue. An optimization of the box size may be required to solve minor problem in the current design and reduce the production cost.

3.3 TOLM:

As described in [2,3,4], this is a PMC mezzanine that provides the following features:

- 2 optical receiver and emitter that could be equipped with single-mode or multi-modes (for communications up to 3.5 km) components. The speed of each link is 2 Gbit/s. These data could be send/received to the two DSP link ports or the PCI interface (initially 32 bits; 33 MHz).
- Interrupt capability on the PCI bus with master capability
- Timing signal generation with an onboard stable clock (Thermal Compensated Crystal Oscillator, TCXO) stabilized using an external 1PPS signal
- Absolute timing information using input IRIG-B frames. These information will be embedded in the data packet.
- Mezzanine Configuration using the PCI bus.

The Figure 7 presents a schematic view of these main functionalities of the TOLM module. The development of the TOLM started in 2004 and the first prototype (see Figure 8) were available at the end of 2004.

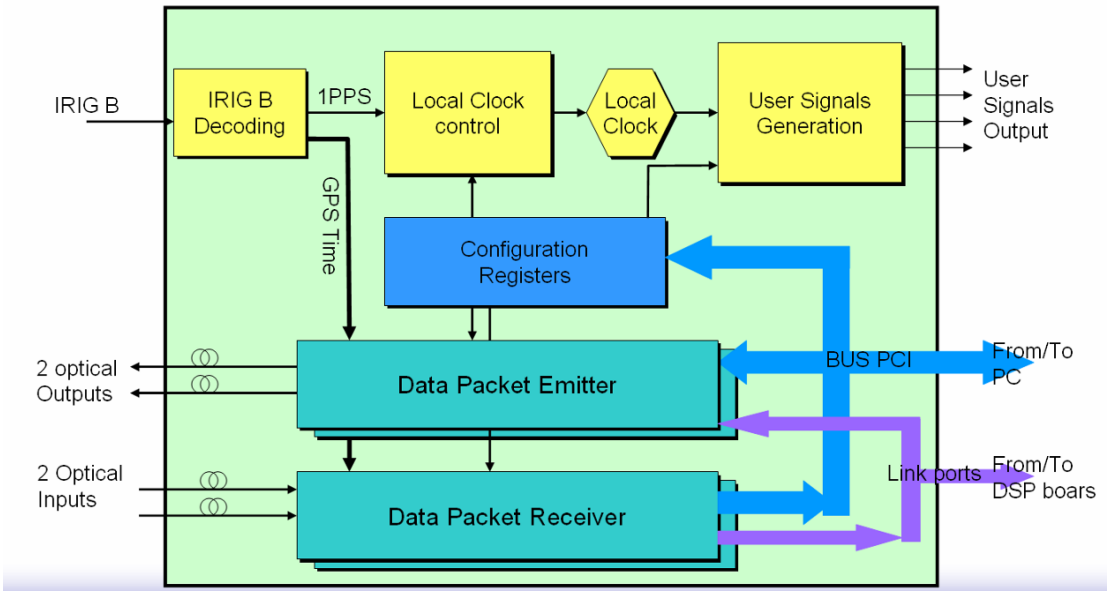

Figure 7 Schematic view of the TOLM

The core of such a module is the FPGA were all the logic for the data transfer and signal generation is implemented. The development of the "software" was one of the main task of 2005 and early 2006. It continues in parallel with the integrations tests. These modules have been used for the software development test presented latter on as well as the ADC development. These results will be presented later in this document.

A new version of the TOLM is foreseen for December 2006 with the following improvements (up to now):

- A larger FPGA to accommodate more functionalities
- The upgrade of the PCI interface to 64 bits, 66MHz.

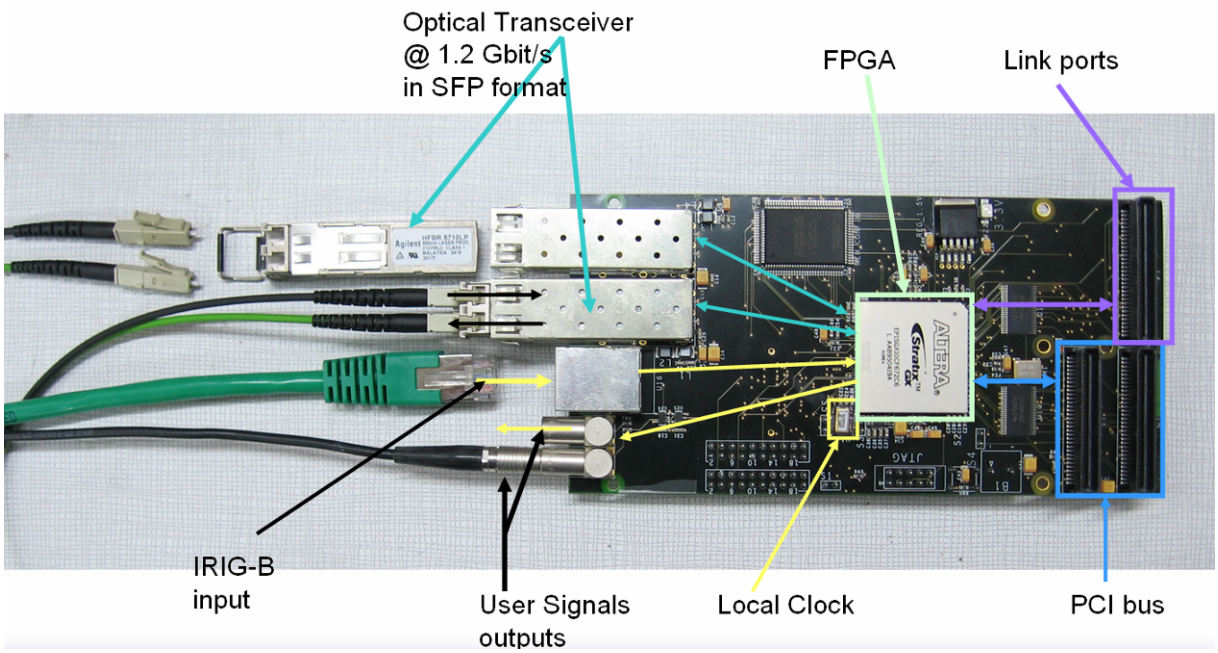

Figure 8 Photo of a TOLM with the input/output presented

The development of the TOLM required the setting up of various tools.

- A PCI bus analyser/exerciser has been purchase to check the PCI and perform different tests.
- A boundary scan board that check all the electrical connections has been developed and build [7].
- A LabView based software to configure the various registers and perform some test has been also developed. (see Figure 9)

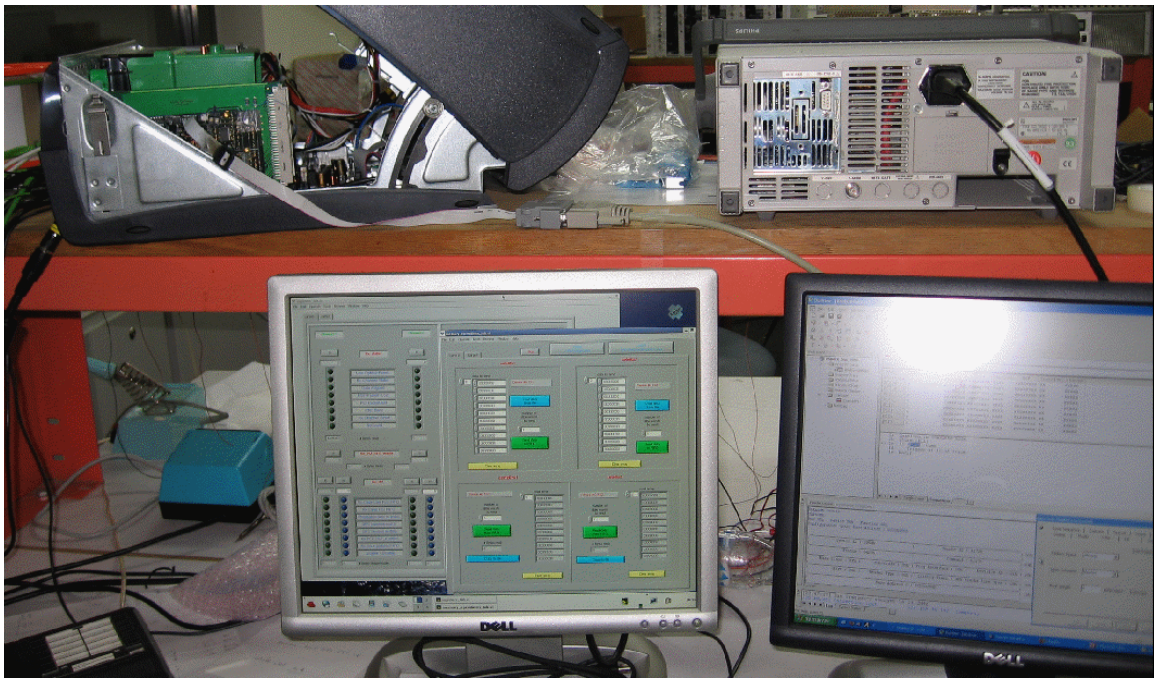

Figure 9 The TOLM mezzanine in a PC with the labview interface (left) and PCI bus analyzer GUI (right)

3.4 Mux/DMux board.

This module is used to group signal coming from different inputs (like multiple photodiodes) to one single output (like the global control) or to go form one input to multiple outputs (like global control to the various suspension control). Eight inputs and outputs optical fibber are available in this board which in fact act as a router since each packet could ask it's own destination.

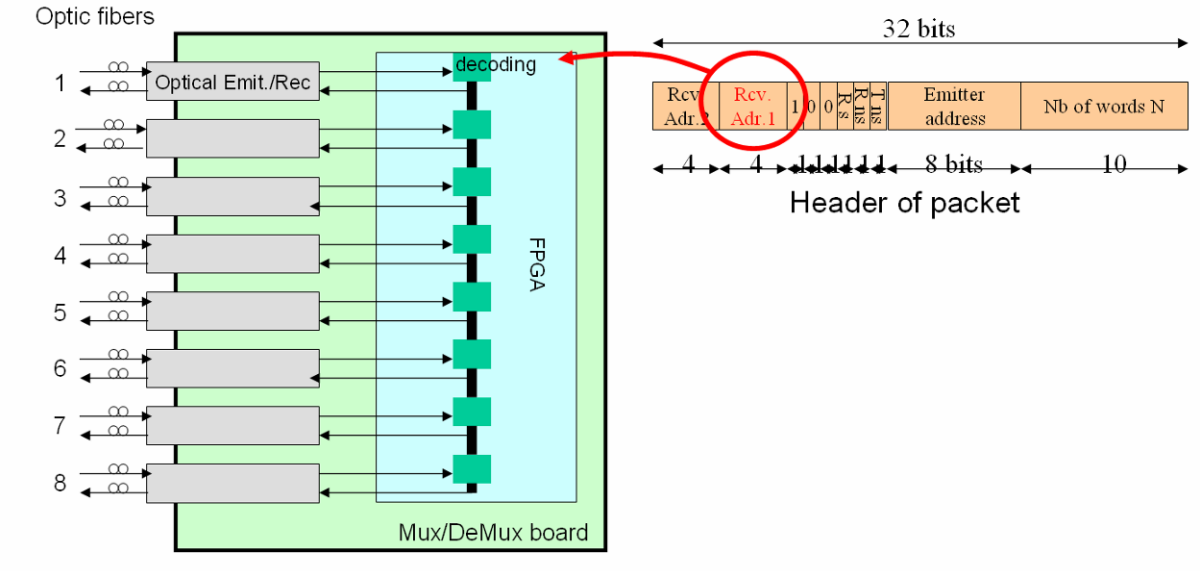

Figure 10 Schematic view of the MUX/DeMUX board and of the basic data packet header.

The specifications have been written in 2005 [6] and the development of the electronic layout completed in early June. The first PCB is expected for the end of June. The cabling of realization of the prototype is expected for end of August.

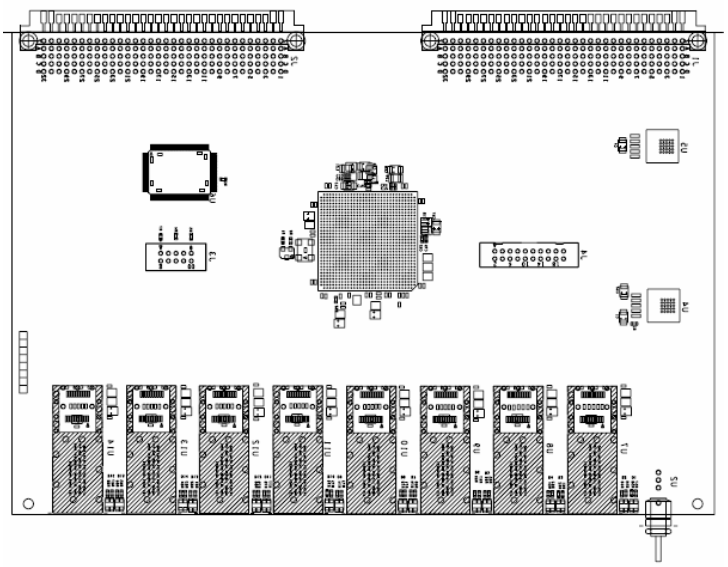

Figure 11 Layout of the MUX/DeMUX board. The 8 optical components and the FPGA are the main elements.

3.5 ADC

Virgo uses now 16 bits ADCs with a sampling rate up to 20 kHz. The goal of this development is to provide new ADCs with:

- A lower noise floor achieved by more bits and/or a faster sampling rate
- A faster sampling rate (a few hundred kHz) to be able to acquire faster channel when debugging some of the analog loop like the frequency stabilization loop and possibly providing input for faster control loops.
- A faster communication channel than the VME.
- A common design to replace the 3 types of ADC used in Virgo.
- New non obsolete components (maintenance issue).
- More compact readout (the ADC used for the photodiode readout take 2 VME slots for 4 channels).
- The possibility to do some on board analog shaping and digital low pass filters

Our low latency constrains of our system push us to make a custom board design with a direct TOLM interface. The use of an optical connection between the ADC module and the processor (PC or DSP) gives use also the benefit of a good behavior for the electromagnetic noise point of view.

This work started by a survey of the existing ADC chip. Once the delta sigma ADCs were removed, only a few possible chip exist. They are:

- Texas Instruments ADS8412 16-bit 2MHz
- Texas Instruments ADS8382 18-bit 600KHz
- Analog Devices AD7621 16-bit 3MHz
- Analog Devices AD7641 18-bit 2MHz
- Analog Devices AD7674 18-bit 800KHz

We then order a few test samples to evaluate their effective performances. To do these measurements, the ADC evaluation board where interfaced to a TOLM modules which send the ADC data to an optical fiber. These data are then collected by PC hosting a TOLM which format the data in regular frames and written them on disk (see Figure 12). Then all the usual Virgo software could be used to handle these data.

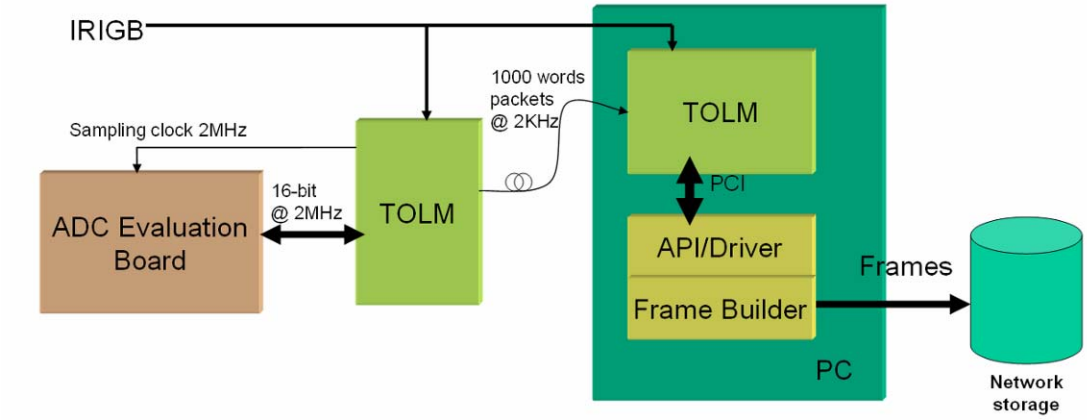

Figure 12 Schematic of the ADC-TOLM data acquisition test bench

Beside the ADC test, it is worth stressing that this is a first integration test were the TOLM are used as a tool. Getting good data (like observing a sine wave) is another test that validates the TOLM.

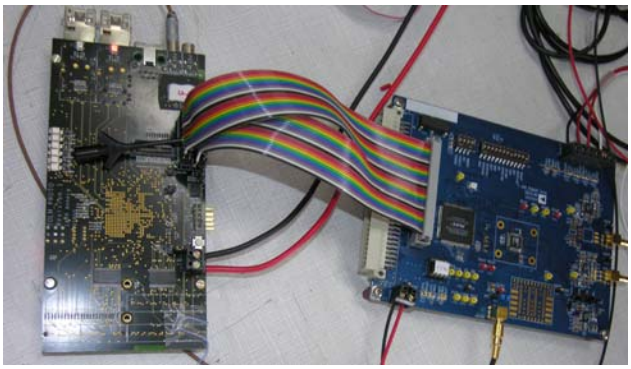

Figure 13 Test of the ADC AD7674

Up to now, the ADC ADS8412 and AD7674 have been tested. The first results obtained are presented in Figure 14. Our current ADCs have a 10^{-6}V/sqrt(Hz) noise floor with a +- 10 V dynamic. These new ADCs have only a +- 5 Volts dynamic. When taking into account this factor we see that we gain about one order of magnitude on the noise floor, thanks to the over sampling of the data.

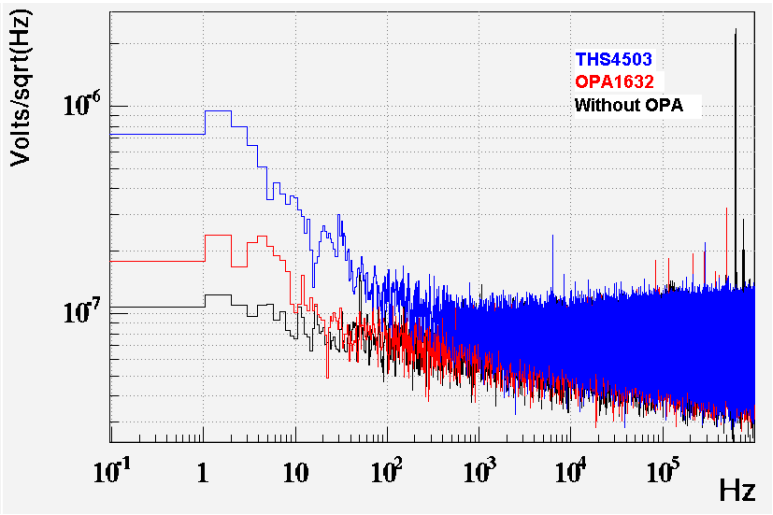

Figure 14 Result of the ADS8412 test with different input amplifier. The noise floor is about 10^{-7}V/sqrt(Hz)

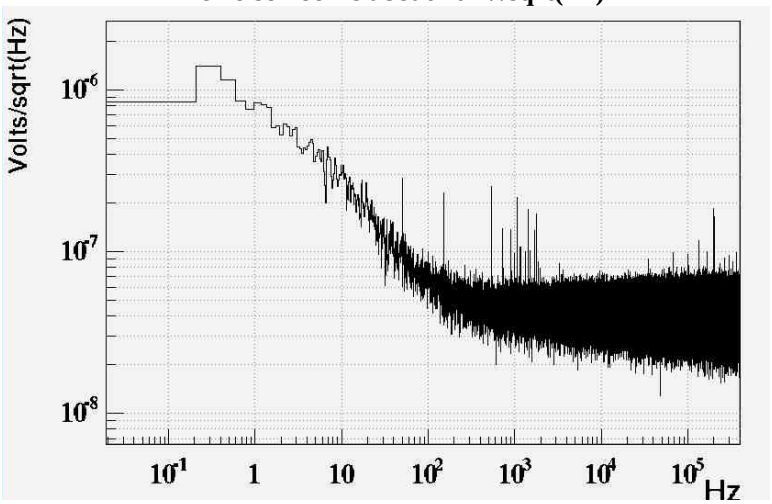

Figure 15 Result of the AD7474 test (18 bits sampled at 800 kHz). The noise floor is around 5.10^{-8}V/sqrt(Hz)

The last samples are expected to be tested by the end of July. Then the layout of the board will start with the goal to get a prototype by the end of November.

3.6 Analog Conditioning board

About 700 ADC channels are collecting the Virgo data with signal with very different dynamic or frequency components. In several cases, the ADC noise is the limitation (especially at high frequency) for channels like the DC photodiode readout, coil current measurement. Therefore we develop an analog module that provides these compression filters as it is already done for the demodulated photodiode signals.

This module (see Figure 16) is a two channel board with 4 different filter and could accept differential or single ended signals. The module has been developed in 2004-05, tested and 30 boards produced. Part of them are now installed in Virgo.

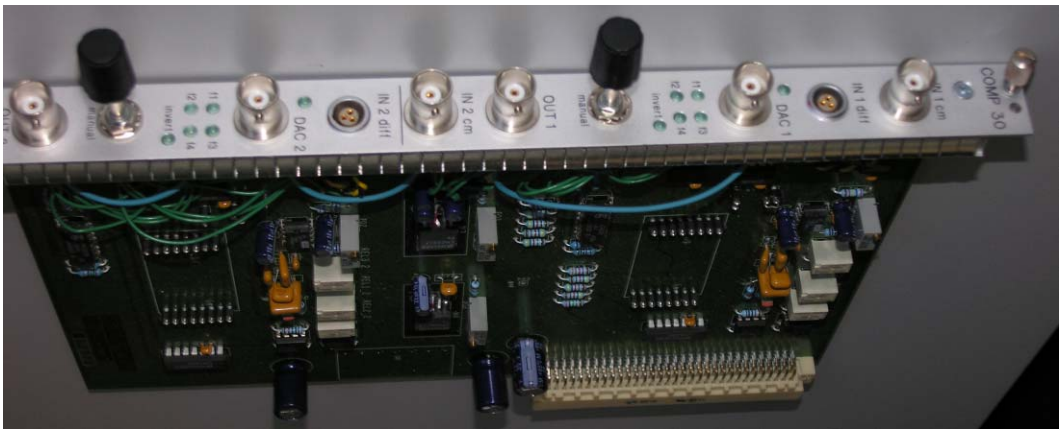

Figure 16 Photo of an analog conditioning board

3.7 Demodulation board

The R&D program foresee a development of new demodulation board that would provide more programmable features (like the compression filter and gain). A differential output that would match the new ADC boar is also expected.

The full development of the new demodulation board did not take place. However, as a temporary solution, 6 existing board were upgraded to include some of the programmable le filter developed for the analog conditioning board. Three of them are now installed in Virgo.

3.8 Software development

The Virgo real time system currently use VME CPUs running LynxOS and DSPs. In this development we want to investigate the replacement of the VME CPUs by plain PCs running a real time version of Linux as well as develop test programs.

Different type of software developments took place. They all use Linux as basic operating system, and quite often the real time version RTAI. Part of the work was to configure different PC under this operating system. Single and dual processors were used to explore the possibility with RTAI.

The first software development was to provide a basic test program for the TOLM. This is the labview interface that has already been quoted in the TOLM section.

Then we develop a program to test the data transfer between the TOLM and the PC. In that case, the TOLM produces interrupt at a given frequency and is acting as a master on the PCI bus for the data transfer. A rate of 0.8 Gbits/s was achieved with the 32 bits interface running at 33 MHz (192 32 bits words in 7 µs). Going to 64 bits and 66 MHz should give us a 3.2 Gbits/s rate, which is one and half time faster that the optical fiber rate.

This development has then evolved to the collection of data from the TOLM for the ADC test previously described.

The last set of development was to investigate the use of Linux PCs for the real time control of Virgo. The developments were made on a dual Xenon processor from Dell running at 3.2GHz. *LINUX SL4* with a kernel 2.6.15-rtai-3.3 was used. The effective interrupt response time was measured in different condition (see Figure 17 and Figure 18). In all cases, the time was frozen at the beginning of the interrupt cycle, and then the processor read the timing counter of the TOLM to measure the effective elapsed time. A typical value of 2 to 3 µs was measured.

In this kind of exercise, the critical parameter is not only the mean response time but also the maximum value since the tail of the distributions could have a dramatic impact on the controls. However, the jitter on the interrupt response time is low enough to foresee an increase of the current 10 kHz main frequency loop.

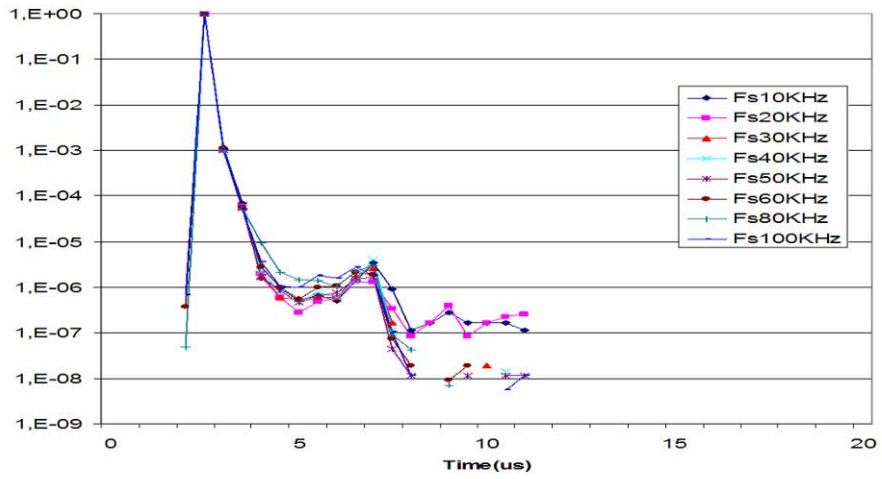

Figure 17. Interrupt response time for different clock frequencies (10 kHz to 100 kHz). The typical acquisition time is half an hour.

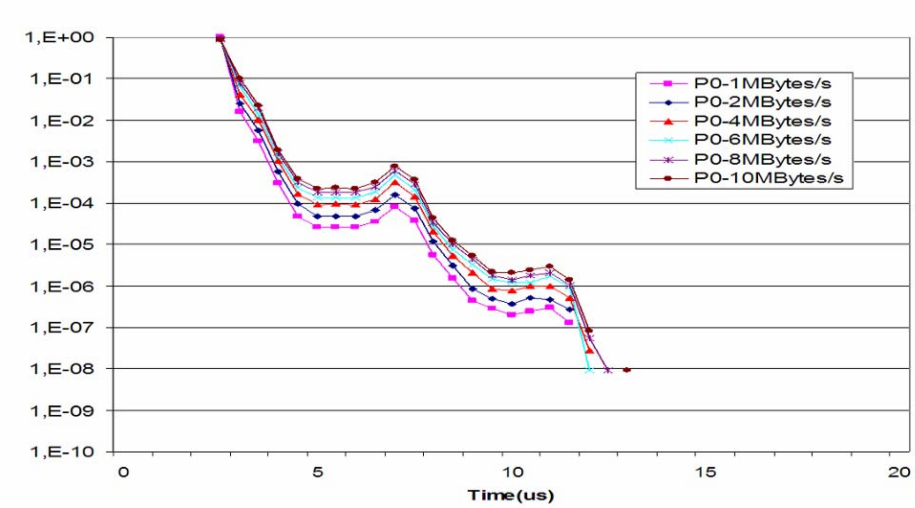

Figure 18 Interrupt response time according the extra load on the PC. The interrupts are generated at 60kHz. The tail of the response is weakly affected by a load of up to 10 MBytes/s on the Ethernet interface.

The Figure 19 present a more realistic condition where the measure cycle do not include just the interrupt response time but also the data transfer on the PCI bus (read and write) and data transfer were performed at the same time on the network interface of the PC. We should stress that the future version of the TOLM will have a faster PCI bus which will reduce the average time.

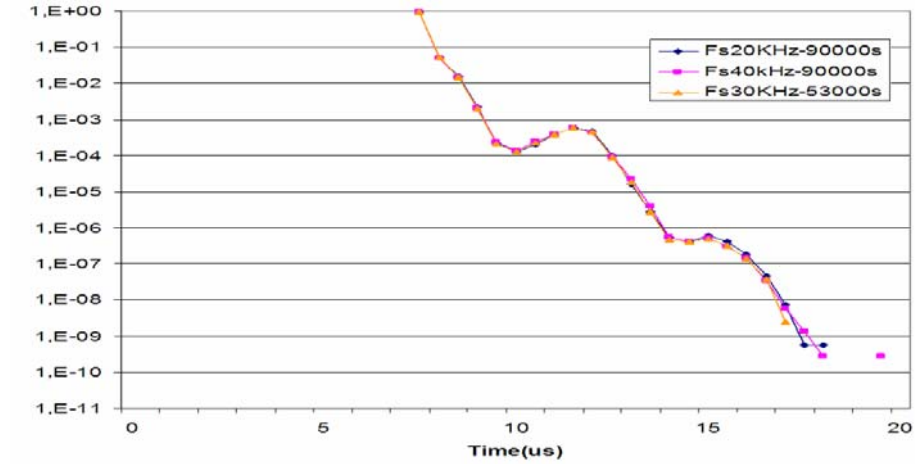

Figure 19 Interrupt response when reading 200 words in the PCI and writing 32 words at each cycles. 10 Mbytes/s are also transfer on the Ethernet interface at the same time. There is no difference between the measurement made at 20, 30 or 40 kHz. The total measurement time is 3 days

These developments and tests will continue with the porting of the full photodiode readout application in this environment. It also includes the development of shared memory tools to bring the data collected at the kernel level to the user level. This will be use for the direct production of data for the data acquisition.

3.9 Conclusions

Although not all the prototype are available the basic components of all the system have been tested and we achieved the following results:

- A factor 10 increase of data rate on the optical fiber and on the bus used by the computing elements (CPU and DSP)
- A full distribution of the GPS time
- A factor 10 reduction of the noise floor for the ADC
- Better analog modules

Therefore we have demonstrated that the technical solutions exist for the upgrade of the Virgo electronic (at least the digital part).

4 Perspectives

[Describe the future of this research]
[Illustrate the benefit to gravitational wave detection and a possible timescale for its application on a existing/planned/envisaged detector]

The prototypes of the MUX/DeMUX and ADC board still need to be completed. This will open the door for a more complete integration test before agreeing on the final design of the components. Critical to perform in the coming weeks/months are

- The interface between the TOLM and the DSP developed by EGO/Pisa
- The communication between the TOLM and the DAC developed by EGO/Pisa

In parallel, the software development will continue to make this test as realistic as possible. Then we will be in position to define the details of the architecture (number of boards; location and type of the computing element) to start the production next year.

The final goal is to install this electronic upgrade during the Virgo+ shutdown of 2008.

5 Use of funds

[Give the usage of the allocated funds listing the expenditures supported]

Expenditures	*Cost (k€)*
Development of Analog conditioning board (30 boards)	*10940*
Development of 6 demodulation boards with variable compression filter	*2900*
Ordering of a test master clock	*8153*
Development of the first prototype of the TDBox	*5530*
Development of the TOLM mezzanine. This including some general test tools like a bus analyzer for 16450 Euros, various IP for PCI (6167 Euros), PCs, and 3 months of a technician)	*43376*
ADC samples	*372*
IN2P3 Overhead; This is 5% of the 155 kEuros allocated up to now. The go back to the lab and are used to pay the internal invoice for the electronic shop (small components).	*7711*
Total 1	***78982***
Fellowship to support the R&D development (S. Karkar; 2 years)	*74000*
Total with the Fellowship	***152982***

Remarks:

- Number are from the end of May 2006
- Only 155 k€ of the initial 180 k€ have been allocated up to now (excluding the post doc position)
- Since this R&D is not over, the remaining fund will be use to complete the development and cover some of the production cost.

6 Publications

List of technical notes available on-line on the Virgo server

1. Consequence of the jitter noise on ADC readout; D. Tombolato; VIR-NOT-LAP-1390-274 (3/08/04)
2. Control System Upgrade of the VIRGO interferometer. Timing Interface & Optical Links; O. Chautemps, et al. VIR-NOT-LAP-1390-278 (11/08/04)
3. Preliminary Timing system interface requirements; O. Chautemps, et al. VIR-NOT-LAP-1390-280 (11/08/04)
4. Proposal for the Timing & Optical Links Mezzanine (TOLM); O. Chautemps, et al. VIR-NOT-LAP-1390-281 (11/08/04)
5. Connectors pin-out of the TOLM ver1.0 prototype; N. Letendre, O. Chautemps; VIR-NOT-LAP-1390-281 (14/09/04)
6. MUX/DEMUX optical card specifications; N. Letendre, VIR-NOT-LAP-1390-321 (15/03/06)
7. TOLM Boundary Scan Board specifications, N. Letendre VIR-NOT-LAP-1390-322 (05/04/06)
8. New timing distribution system for Virgo: prospect for a full system from the market; S. Karkar. June 9, 2006, VIR-NOT-LAP-1390-323