Test Procedure

ISYS DC Quadrant Photodetector Board

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1   Overview

The following procedure refers to the validation of the ISYS DC QPD (DYYMMnn-Rev-Ver). This board implements the analog processing electronics for the Beam Monitor System and the Input Mode Cleaner Quadrant PhotoDiodes (QPD).
Each unit consists of one processing and one sensor board, hosted in a 121x95x61 mm metallic box. The sensor (UDT SPOT-15-YAG) is mounted on the latter. The output current of every quadrant is available on the processing pcb through a 4-pin connector (J8).

The tests presented here aim at validating the processing board (QPD electronics) in all its features and characteristics, which go beyond the ones requested for working in the field once the box hosting the boards mentioned has the lid on. In the condition just mentioned only a subset of these features will be available.

In what follows it is assumed that the board is correctly mounted in its own box which in turn is completely assembled. The lid instead has been removed (and the LEDs on it disconnected).

In the condition described, once the board is correctly oriented (i.e., the wording on the board's silkscreen is) the box has two switches on the left side and 7 connectors on the top of the box. The sensor board remains on the right.

The *PWR Switch* is used to bring the electronics in working condition, the second one instead (*Int Dignostic PWR*) allows to power the diagnostic section of the board. It is kept off when the box is close.

The BNC connectors are either for monitor or test input, the 3-pin LEMOs are used either to supply power to the electronics or to acquire board outputs.

2   Test Equipment

To test the QPD board it is necessary to use the following pieces of equipment:

Dual DC power supply (capable of ± 24 Vdc), with the additional fixed +5 Vdc output
Dual Channel Scope with scope probes
Dynamic Signal Analyzer (for example, Ono-Sokki CF-6400 or Stanford Research SR785)
3-pin LEMO to BNC adapter[1]
Function Generator (for example, Agilent 33220A) capable of going below 100 mHz

If the DSA is not available, for transfer function measurement a combination of Scope and the Function Generator just mentioned can be used instead.

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[1] small black box available in the EE Shop. Third pin *not* connected to ground

3 Test Setup

Apply ± 24 Vdc and Ground using the 3-pin LEMO connector on the left of the box, labelled PWR, according to the pinout indicated.

Alternatively, it is possible to use clip leads connecting them to the test points TP4 and TP5 labelled +24PS, –24PS respectively. Use another clip lead to connect the GND test point TP2 to the common point of the power supply.
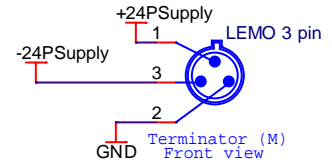
In what follows the conditions in which the measurements are to be taken are always specified.

4 Test Overview

The functional tests described below are used to verify the correct operation of the QPD board.

Input Power level

This test will verify that the QPD board draws the proper amount of current from the power supply.

Algebraic Functions

These tests will verify that the algebraic functions implemented by the various stages are the ones expected:

X = Q1+Q4 – (Q2+Q3)   Y = Q1+Q2 – (Q3+Q4),   SUM = |Q1+Q2+Q2+Q4|

Beam Position/Threshold Detection

These tests will verify that in response to an equivalent position of the beam that moves away from the centre of the sensor, an "over-threshold" situation is detected and, correspondingly, one or more LEDs go off.

Transfer Functions

These two tests will verify the proper behaviour of the first order high pass filters specified in par 5.4.

Monitor and DAQ signals integrity

These tests will verify that signals available for the DAQ and as monitor on the board BNC output are an accurate replica of the computed ones.

Output Referred Noise

This test will verify the proper noise level as measured at the 3 monitor outputs of the board.

Those test can be grouped together to simplify the test procedure.

5 Test Procedure (Stand alone mode)

The following tests are performed *with no sensor connected* to the processing board. Both power switches have to be ON.

5.0 Jumpers default positions

JP14-**12**   JP15-**12**   ("to the right" position)

5.1 Input Power

Supply	Nominal Current	Measured Current	Check if OK
-24 V	100 mA (± 20 mA)		☐
+24 V	100 mA (± 20 mA)		☐

5.2 Algebraic Functions

To apply the input voltage, emulating the behavior of a single quadrant at the time, it is useful to use the feature offered by U3, located at bottom right corner of the board, which allows to selectively inject Test Signals "Test Qn", with n = 1, 2, 3, 4.

The default position for U3's contacts is the one shown (all "on the left") which corresponds to all open

The voltage source used is the +5 Vdc level available on the Bench Power Supply mentioned above. Please note that to reproduce correctly the voltage signs it is necessary to inject a negative voltage (i.e., connect to the power supply ground the +5V output and use its negative contact as input to the board under test).

Apply +5 Vdc and Ground through a voltage divider as shown[2] using the BNC connector Analog IN, on the top of the box according to the pinout indicated.

Alternatively, it is possible to use a clip lead connecting it to the test points TP6 labelled Test In. Do not forget to connect the positive +5 Vdc output of the Power Supply to the common point of the ± 24 Vdc power supply.

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[2] the voltage divider mentioned is available in a conveniently packaged box in the EE Shop, but it can of course be easily built on the spot

Input	U3 contact positions				test In TP5	X Mon	Y Mon	SUM Mon	LED bars ON	
					Output Voltage [V]					
BNC Analog IN	1 off	2 off	3 off	4 off	0	<0.16	<0.16	<0.01		☐
	1 **ON**	2 off	3 off	4 off	-2.5	+2.5	+2.5	+2.5	2	☐
	1 **ON**	2 **ON**	3 off	4 off	-1.8	0	+3.7	+3.7	3	☐
	1 **ON**	2 **ON**	3 **ON**	4 off	-1.4	-1.4	+1.4	+4.4	4	☐
	1 **ON**	2 off	3 **ON**	4 **ON**	-1.4	+1.4	-1.4	+4.4	4	☐
	1 off	2 off	3 **ON**	4 **ON**	-1.8	0	-3.7	+3.7	3	☐

5.3 Beam Position/Threshold Detection

Goal of this test is to verify that the stages driving the LEDs used to manually align the detector (when the lid is on) can work as designed.

X

Input	U3 contact positions	Output Voltage J10 [V]		Output Voltage J10 [V]		LED bars ON
		pin1	pin4	pin2	pin3	
BNC Analog IN	1 **ON** 2 off 3 off 4 off	-4.0	-4.0	0	0	2

Reverse Input voltage polarity and repeat

Input	U3 contact positions	Output Voltage J10 [V]		Output Voltage J10 [V]		LED bars ON
		pin1	pin4	pin2	pin3	
BNC – Analog IN	1 **ON** 2 off 3 off 4 off	+4.0	+4.0	0	0	0

Y

Input	U3 contact positions	Output Voltage J10 [V]		Output Voltage J10 [V]		LED bars ON
		pin1	pin4	pin2	pin3	
BNC – Analog IN	1 **ON** 2 off 3 off 4 off	-4.0	-4.0	0	0	2

Reverse Input voltage polarity and repeat

Input	U3 contact positions	Output Voltage J10 [V]		Output Voltage J10 [V]		LED bars ON
		pin1	pin4	pin2	pin3	
BNC – Analog IN	1 **ON** 2 off 3 off 4 off	+4.0	+4.0	0	0	0

SUM

Input	U3 contact positions	Output Voltage J5-pin1 ("left")[V]	Output Voltage J5-pin2 ("right") [V]	LED bars ON
BNC – Analog IN	1 **ON** 2 off 3 off 4 off	-2.5	0	2

Reverse Input voltage polarity and repeat

Input	U3 contact positions	Output Voltage J5-pin1 ("left")[V]	Output Voltage J5-pin2 ("right") [V]	LED bars ON
BNC –Analog IN	1 **ON** 2 off 3 off 4 off	+2.5	0	0

5.4   Filter time response / Transfer Function

The Dynamic Signal Analyzer, used together with the scope (to avoid taking measurements affected by saturation), allows to measure the various transfer functions to asses the proper behaviour of the board under test.

If not available, a rougher estimate of the correct behavior can be obtained using a signal generator and a dual channel scope

1) X TF

Input	Output	U3 contact positions	Vsource	Frequency Span
BNC –Analog IN	TP10	1 **ON** 2 off 3 off 4 off	100 mV	250 mHz – 200 Hz
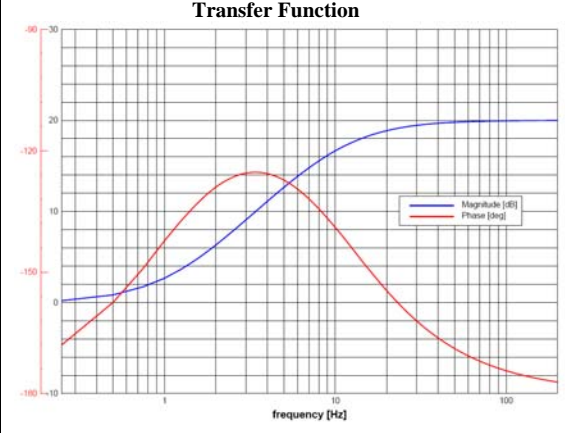
Freq (Hz)	Nominal values	Measured values	Check if OK	Transfer Function
0.5	Gain (dB) 0.95 ± 0.5	Gain (dB)		
	Phase (deg) -156.3 ± 3	Phase (deg)		
3.5	Gain (dB) 10.7 ± 1	Gain (dB)		
	Phase (deg) -125 ± 3	Phase (deg)		
38	Gain (dB) 19.75 ± 1	Gain (dB)		
	Phase (deg) -167 ± 3	Phase (deg)		
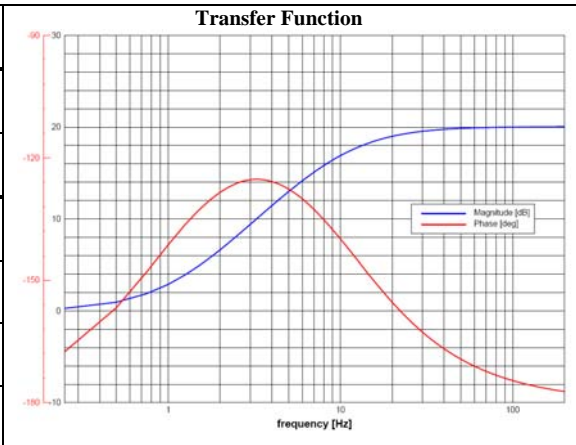
2) Y TF

Input	Output	U3 contact positions				Vsource	Frequency Span
BNC –Analog IN	TP9	1 **ON**	2 off	3 off	4 off	100 mV	250 mHz – 200 Hz

Freq (Hz)	Nominal values	Measured values	Check if OK	Transfer Function
0.5	Gain (dB) 0.95 ± 0.5	Gain (dB)		
	Phase (deg) -156.3 ± 3	Phase (deg)		
3.5	Gain (dB) 10.7 ± 1	Gain (dB)		
	Phase (deg) -125 ± 3	Phase (deg)		
38	Gain (dB) 19.75 ± 1	Gain (dB)		
	Phase (deg) -167 ± 3	Phase (deg)		

5.5 Monitor and DAQ signal integrity

The goal is to verify that the output stages of the board are behaving as expected.

The test consists in injecting a known DC voltage level and check that amplitudes and signs are correct.

The voltage input is still the same +5 Vdc power supply used in par 5.2, again with reversed polarity, the output will be measured whenever possible putting to use the connectors available and explicitly indicated, otherwise it is suggested to remove the cabling going from the bulkhead connectors to the mating ones on the pcb and measure on the corresponding pins (indicated below).

X Pos DAQ

Input	Output	Nominal value	Measured value	Check if Sign OK	Check if Amplitude OK
BNC Analog IN	DAQ X-pin1 (equivalent to J13-pin1)			☐	☐
BNC Analog IN	DAQ X-pin3 (equivalent to J13-pin3)			☐	☐

X Mon

Input	Output	Nominal value	Measured value	Check if Sign OK	Check if Amplitude OK
BNC Analog IN	Mon X-pin1 (equivalent to J17-pin1)			☐	☐

Y Pos DAQ

Input	Output	Nominal value	Measured value	Check if Sign OK	Check if Amplitude OK
BNC Analog IN	DAQ Y-pin1 (equivalent to J12-pin1)			☐	☐
BNC Analog IN	DAQ Y-pin3 (equivalent to J12-pin3)			☐	☐

Y Mon

Input	Output	Nominal value	Measured value	Check if Sign OK	Check if Amplitude OK
BNC Analog IN	Mon X-pin1 (equivalent to J16-pin1)			☐	☐

SUM Mon

Input	Output	Nominal value	Measured value	Check if Sign OK	Check if Amplitude OK
BNC Analog IN	Mon SUM-pin1 (equivalent to J9-pin1)			☐	☐

5.6 Output Referred Noise

To evaluate the performance in terms of noise it is necessary to use the FFT analyzer

The Change Request document associated with the design and production of this electronics (virchreq0162006) specified, in the most restrictive case, a noise level of 216 pA/sqrt(Hz) at the output of the sensor.
Given the transimpedance of the input stage (3.2 kΩ) this means that the input referred noise of the board under test has to be less than 700 nV/sqrt(Hz).

This requirement is easily satisfied on the SUM channel, given the factor 10 lower gain with respect to the X and Y channels.

Instruments setup
Channel Sensitivity   10 mVr
Sensor disconnected
Test inputs OFF
Box connected to earth (PS)
Shield Connected
Hanning Window

	Output	U3 contact positions				Frequency Span	
X channel	J17	1 off	2 off	3 off	4 off	125 Hz – 100 kHz	☐
Y channel	J16	1 off	2 off	3 off	4 off	125 Hz – 100 kHz	☐
SUM channel	J9	1 off	2 off	3 off	4 off	125 Hz – 100 kHz	☐

X output noise

Y output noise